

CLAIMS

What is claimed is:

1. A method for reducing the contact resistance of metal silicide contacts comprising the steps of:

(a) forming a metal germanium alloy layer over a silicon-containing substrate, wherein said metal is Co, Ti, Ni or mixtures thereof;

(b) annealing said metal germanium alloy layer at a temperature sufficient to convert at least a portion of said metal germanium alloy layer into a metal silicide layer that is substantially non-etchable compared to the unreacted metal germanium alloy layer, while forming a Si-Ge interlayer between said silicon-containing substrate and said substantially non-etchable metal silicide layer;

(c) removing any remaining metal germanium alloy layer, with the proviso that when Ti or Co are employed a second annealing step follows step (c) that is capable of converting the substantially non-etchable Ti or Co silicide phase into Co disilicide or C54 phase of  $TiSi_2$ .

2. The method of Claim 1 further comprising pre-annealing the metal germanium alloy layer prior

3 to step (b) at a temperature sufficient to form  
4 a metal rich germanium silicide layer.

1 3. The method of Claim 1 wherein said metal  
2 germanium alloy layer is formed by a deposition  
3 process selected from the group consisting of --  
4 chemical vapor deposition (CVD), plasma-  
5 assisted CVD, sputtering and evaporation, or  
6 said metal germanium alloy layer is formed by  
7 first depositing said metal to form a metal  
8 layer and then doping said metal layer with  
9 germanium.

1 4. The method of Claim 1 further comprising  
2 forming an optional barrier layer over said  
3 metal germanium alloy layer prior to step (b),  
4 wherein said optional barrier layer is removed  
5 by step (c).

1 5. The method of Claim 1 wherein said metal  
2 germanium alloy layer further includes at least  
3 one additive selected from the group consisting  
4 of C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni,  
5 Cu, Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf,  
6 Ta, W, Re, Ir, Pt, Ce, Pr, Nd, Sm, Eu, Gd, Tb,  
7 Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof.

1 6. The method of Claim 5 wherein said additive is  
2 C, Al, Si, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu,  
3 Y, Zr, Nb, Mo, Ru, Rh, Pd, In, Sn, La, Hf, Ta,  
4 W, Re, Ir, Pt or mixtures thereof

- 1 7. The method of Claim 6 wherein said additive is  
2 Si, Ti, V, Cr, Ni, Nb, Rh, Ta, Re, Ir or  
3 mixtures thereof.
- 1 8. The method of Claim 1 wherein said metal  
2 germanium alloy layer contains from about 0.01-  
3 to about 50 atomic % Ge.
- 1 9. The method of Claim 8 wherein said metal  
2 germanium alloy layer contains from about 0.1  
3 to about 20 atomic % Ge.
- 1 10. The method of Claim 1 wherein said metal of  
2 said metal germanium alloy layer is Co.
- 1 11. The method of Claim 4 wherein said optional  
2 oxygen barrier layer is composed of TiN.
- 1 12. The method of Claim 1 wherein said silicon-  
2 containing substrate comprises a single crystal  
3 Si, polycrystalline Si, SiGe, amorphous Si, or  
4 a silicon-on-insulator (SOI).
- 1 13. The method of Claim 2 wherein said pre-  
2 annealing step is carried out using rapid  
3 thermal annealing (RTA).
- 1 14. The method of Claim 13 wherein said RTA is  
2 carried out at a temperature of from about 350°  
3 to about 450°C for a time period of about 300  
4 seconds or less

- 1 15. The method of Claim 1 wherein said annealing  
2 step (b) is carried out by RTA.
- 1 16. The method of Claim 15 wherein said RTA is  
2 carried out at a temperature of from about 400°  
3 to about 700°C for a time period of about 300 ~  
4 seconds or less.
- 1 17. The method of Claim 1 wherein said remaining  
2 metal germanium alloy layer is removed  
3 utilizing a wet etch step that includes the use  
4 of an etchant that is selective for removing  
5 said layer.
- 1 18. The method of Claim 1 wherein said second  
2 annealing step is carried out by RTA.
- 1 19. The method of Claim 18 wherein said RTA is  
2 carried out at a temperature of from about 700°  
3 to about 900°C for a time period of about 300  
4 seconds or less.
- 1 20. The method of Claim 1 wherein said metal is Ni  
2 and Ni monosilicide is formed after step (b).
- 1 21. The method of Claim 1 wherein said metal is Co  
2 and Co monosilicide is formed after step (b).
- 1 22. The method of Claim 1 wherein said metal is Ti  
2 and C49 phase of  $\text{TiSi}_2$  is formed after step  
3 (b).

1       23.       An electrical contact to a region of a silicon-  
2                   containing substrate comprising:

3                   a substrate having an exposed region of a  
4                   silicon-containing semiconductor material; and

5                   a first layer of metal disilicide, wherein said  
6                   metal of said disilicide is selected from the  
7                   group consisting of Ti, Co and mixtures  
8                   thereof, and said substrate and said first  
9                   layer are separated by a Si-Ge interlayer.

1       24.       An electrical contact to a region of a silicon-  
2                   containing substrate comprising:

3                   a substrate having an exposed region of a  
4                   silicon-containing semiconductor material; and

5                   a first layer of Ni monosilicide, wherein said  
6                   substrate and said first layer are separated by  
7                   a Si-Ge interlayer.  
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